the program counter including a first program counter and a second program counter,

the first program counter indicating a storage position of a processing packet in the memory, the processing packet being made of an integer number of bytes, the storage position being a position corresponding to a byte boundary,

the second program counter indicating a position of processing target instruction in the processing packet, the processing target instruction being an operation to be executed by the processor, and the position of which does not correspond to a byte boundary.

10. (Amended) The processor of Claim 1,

wherein the first program counter indicates bits of a memory address more significant than a $1 + log_2 n^{th}$ bit from a least significant, the memory address specifying the storage position of the processing packet in memory, and n being a length of a processing packet in bytes.

Please add the following new claim:

49. (New) A processor for reading instructions from a memory according to a program counter, and for executing the read instruction,

the program counter including a first program counter and a second program counter,

the first program counter indicating a storage position of a processing packet in the memory, the processing packet being made of an integer number of bytes, the storage position being a position corresponding to a byte boundary,

the second program counter indicating a position of processing target instruction in the processing packet, by cycling through m different values, with m not being a power of 2, and sending a carry if the second program counter cycles,

the processing target instruction being an operation to be executed by the processor, and the position of which does not correspond to a byte boundary.